PXE-12S-R10

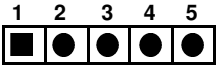
Jun. 06, 2008

12-Slot PICMG 1.3 Backplane

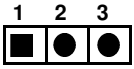
User Manual Ver. 1.0

1. J1 : Intel Bridge 41210 Use MCU read/write Pin

Pin	DESCRIPTION
1	MCLR
2	+5V
3	GND
4	RB7/PGD
5	RB6/PGC



2. J2 & J3 : Intel Bridge 41210 SM-BUS Setting

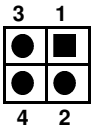


Pin	DESCRIPTION
1-2	Normal Operation (default)
2-3	Test Purposes

3. J4 : Intel Bridge 41210 Initialization Register Setting

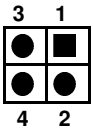
J4	DESCRIPTION
Open (High)	Initialization Register
Short (Low)	Normal response (default)

4. J5 : PCI-X_A1~PCI-X_A4 Frequency Setting



Freq. \ Pin		1 - 2	3 - 4
PCI	33 MHz	Open	Short
	66 MHz (Default)	Short	Open
PCI-X	66 MHz (Default)	Short	Open

5. J7 : PCI-X_B1 & PCI-X_B2 Frequency Setting

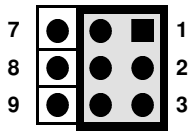


Freq. \ Pin		1 - 2	3 - 4
PCI	33 MHz	Open	Short
	66 MHz (Default)	Short	Open
PCI-X	66 MHz (Default)	Short	Open
	100 MHz	Open	Short

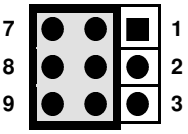
6. VIO_J1 : PCI-X_A1 ~ PCI-X_A4 VIO Power Setting
VIO_J2 : PCI-X_B1 & PCI-X_B2 VIO Power Setting

PCI-X Slot	DESCRIPTION
+5V	1-4 , 2-5 , 3-6 Short
+3.3V	7-4 , 8-5 , 9-6 Short (default)

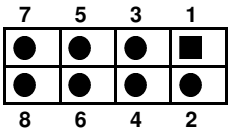
VIO = +5V



VIO = +3.3V



6. USB1、USB2 External USB Connector



PIN	DESCRIPTION	PIN	DESCRIPTION
1	USBVCC	2	GND
3	DATA-	4	DATA+
5	DATA+	6	DATA-
7	GND	8	USBVCC

7. FAN1、FAN2、FAN3、FAN4 : Fan Connector

PIN NO.	DESCRIPTION
1	GND
2	+12V
3	NC

8. ATXCTL1 : Backplane to Mainboard Connector

PIN NO.	DESCRIPTION
1	GND
2	PSON#
3	5VSB

9. PWRBTN : Power on Button

PIN NO.	DESCRIPTION
1	GND
2	PWRBT#

10. RESET : Reset Button

PIN NO.	DESCRIPTION
1	GND
2	SHB_RST#

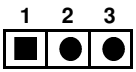
11. PWRGD : Power Good Connector

PIN NO.	DESCRIPTION
1	GND
2	PWRGD

12. SM-BUS : System Management BUS Connector

PIN NO.	DESCRIPTION
1	SMDAT
2	SMCLK

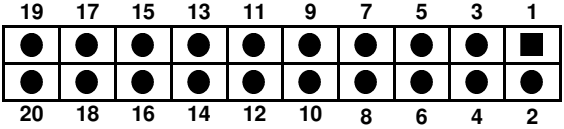
13. CN1 : PCIE X8 SDVO Control Signal Pin



PIN NO.	DESCRIPTION
1	EXP_EN
2	SDVO_CLK
3	SDVO_DAT

14. IOPWR : I/O Power Connector

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	-12V
3	+12V	4	GND
5	IPMB_DA	6	5VSB
7	GND	8	GND
9	IPMB_CL	10	5VSB
11	+5V	12	PWRGD
13	SMDAT	14	SHB_RST#
15	5VSB	16	GND
17	SMCLK	18	PSON#
19	+3.3V	20	PWRBT#



15. PCI routing table:

PICMG1.3 Local PCI routing table :

SIGNAL	REQ#	GNT#	IDSEL	INTA#	INTB#	INTC#	INTD#
PIN No.	B18	A17	A26	A6	B7	A7	B8
PCI1	REQ0#	GNT0#	AD31	B	C	D	A
PCI2	REQ1#	GNT1#	AD30	C	D	A	B
PCI3	REQ2#	GNT2#	AD29	D	A	B	C
PCI4	REQ3#	GNT3#	AD28	A	B	C	D

PCI Express to PCI-X Group A routing table :

SIGNAL	REQ#	GNT#	IDSEL	INTA#	INTB#	INTC#	INTD#
PIN No.	B18	A17	A26	A6	B7	A7	B8
PCI-X_A1	REQ0#	GNT0#	AD28	A	B	C	D
PCI-X_A2	REQ1#	GNT1#	AD29	B	C	D	A
PCI-X_A3	REQ2#	GNT2#	AD30	C	D	A	B
PCI-X_A4	REQ3#	GNT3#	AD31	D	A	B	C

PCI Express to PCI-X Group B routing table :

SIGNAL	REQ#	GNT#	IDSEL	INTA#	INTB#	INTC#	INTD#
PIN No.	B18	A17	A26	A6	B7	A7	B8
PCI-X_B1	REQ0#	GNT0#	AD28	A	B	C	D
PCI-X_B2	REQ1#	GNT1#	AD29	B	C	D	A

15. Notice:

a. **Recommend to use 6mm width spacer to install**

b. **Torsion must less than 6lb-inch**

c. **The voltage settings of the green jumper keys of the PCI-X slots must be the same with the voltage settings of the VIO Power jumper (VIO_J1,VIO_J2). Incorrect usage may cause permanently damage to the backplane and CPU card.**

16. Dimension: